In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims.

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A bipolar transistor of NPN type implemented in an epitaxial layer within a window defined in a thick oxide layer, including:

an opening formed substantially at the center of the window, the opening penetrating into the epitaxial layer down to a depth of at least the order of magnitude of the thick oxide layer, the walls of the opening being coated with a layer of silicon oxide and with a layer of silicon nitride,

a polysilicon spacer formed on the lateral walls and a portion of the bottom wall of the opening,

an N-type highly-doped polysilicon layer formed in the opening and in contact with the epitaxial layer at the bottom of the opening within the space defined by the spacer,

an N-type doped region at the bottom of the opening,

a first P-type doped base region at the bottom of the opening,

a second lightly-doped P-type region on the sides of the opening, and

a third highly-doped P-type region formed in the vicinity of the upper part of the opening, this third region being in contact with [[an N-type]] a P-type doped polysilicon layer, the three P-type regions being contiguous and forming the base of the transistor.

2. (Original) An NPN transistor according to claim 1, further including a fourth P-type doped intermediary region between the third and second regions.

3. (Original) An NPN transistor according to claim 1, having a collector is formed vertically of a portion of the epitaxial layer, of an overdoped region resulting from an implant in the opening and of a buried layer.

4-9. (Canceled)

10. (Previously presented) A bipolar transistor formed in an epitaxial layer of a first conductivity type disposed on a semiconductor substrate of a second conductivity type, the bipolar transistor being formed within a window defined in a thick oxide layer that is disposed above the epitaxial layer, the bipolar transistor comprising:

an opening formed substantially at a center of the window, the opening penetrating into the epitaxial layer, the opening being defined by lateral walls at lateral sides of the opening and a bottom wall at a bottom of the opening;

a first region of the second conductivity type formed in the epitaxial layer along the bottom wall of the opening;

an insulating layer coating the lateral walls and a portion of the bottom wall of the opening;

a polysilicon spacer formed on the insulating layer coating the lateral walls and the portion of the bottom wall of the opening;

a polysilicon layer of the first conductivity type formed in the opening and contacting the polysilicon spacer and the bottom wall of the opening within a space defined by the polysilicon spacer;

a second region of the first conductivity type formed in the first region and contacting the polysilicon layer along the bottom wall of the opening within the space defined by the polysilicon spacer;

a third region of the second conductivity type formed in the epitaxial layer along the lateral sides of the opening and contacting the insulating layer and the first region; and

a fourth region of the second conductivity type disposed on the epitaxial layer within the window and surrounding the opening at an upper portion of the opening.

11. (Previously presented) The bipolar transistor of claim 10, wherein the first, third and fourth regions form a base of the transistor.

12. (Previously presented) The bipolar transistor of claim 10, further comprising a fifth region of the second conductivity type formed in the epitaxial layer along the lateral sides of the opening and contacting the third and fourth regions, the fifth region, together with the first, third, and fourth regions forming a base of the bipolar transistor.

13. (Previously presented) The bipolar transistor of claim 12, wherein a doping level of the fifth region is between a doping level of the first region and a doping level of the fourth region.

14. (Previously presented) The bipolar transistor of claim 12, wherein the fifth region is frusto-conically shaped.

15. (Previously presented) The bipolar transistor of claim 12, wherein the second region and the polysilicon layer form an emitter of the bipolar transistor.

16. (Previously presented) The bipolar transistor of claim 15, further comprising a buried layer of the first conductivity type buried in the epitaxial layer below the first and second regions, the buried layer forming a collector of the bipolar transistor.

17. (Previously presented) The bipolar transistor of claim 16, wherein the polysilicon layer of the first conductivity type is a highly doped polysilicon layer of the first conductivity type.

18. (Previously presented) The bipolar transistor of claim 16, wherein a depth of the opening is a same order of magnitude as a thickness of the thick oxide.

19. (Previously presented) The bipolar transistor of claim 18, wherein the depth of the opening is between approximately 300 and 1000 nm.

20. (Previously presented) The bipolar transistor of claim 10, wherein a depth of the opening is a same order of magnitude as a thickness of the thick oxide.

21. (Previously presented) The bipolar transistor of claim 20, wherein a width of the opening is approximately one half a width of the window.

22. (Previously presented) The bipolar transistor of claim 10, wherein a width of the opening is approximately one half a width of the window.

23. (Previously presented) The bipolar transistor of claim 10, wherein the insulating layer includes a silicon nitride layer and a silicon oxide layer.

24. (Previously presented) The bipolar transistor of claim 10, wherein the insulating layer includes a silicon nitride layer disposed upon a silicon oxide layer.

25. (Previously presented) The bipolar transistor of claim 10, wherein the bipolar transistor is implemented within a same semiconductor substrate as a CMOS transistor.

26. (Previously presented) The bipolar transistor of claim 10, further comprising a silicon nitride layer coating a portion of the fourth region that immediately surrounds the opening to prevent the fourth region from contacting the polysilicon layer.